

Docket No. 214890US-2 S

IN RE APPLICATION OF: Hiroshi WATANABE, et al.

SERIAL NO: 09/973,019

FILED: October 10, 2001

FOR: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME



ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Transmitted herewith is an amendment in the above-identified application.

- ☒ No additional fee is required
- ☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
- ☒ Additional documents filed herewith: marked-up copy

The Fee has been calculated as shown below:

CLAIMS	CLAIMS REMAINING		HIGHEST NUMBER PREVIOUSLY PAID	NO. EXTRA CLAIMS	RATE	CALCULATIONS
TOTAL	7	MINUS	20	0	x \$18 =	\$0.00
INDEPENDENT	1	MINUS	6	0	x \$84 =	\$0.00
		<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS			+ \$280 =	\$0.00
		TOTAL OF ABOVE CALCULATIONS				\$0.00
		<input type="checkbox"/> Reduction by 50% for filing by Small Entity				\$0.00
		<input type="checkbox"/> Recordation of Assignment			+ \$40 =	\$0.00
		TOTAL				\$0.00

☐ A check in the amount of **\$0.00** is attached.

☒ Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

☒ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

HIROSHI WATANABE, ET AL. :

SERIAL NO: 09/973,019 :

FILED: OCTOBER 10, 2001 :

FOR: SEMICONDUCTOR DEVICE AND
METHOD OF MANUFACTURING
THE SAME :

#10A Aust
EXAMINER: PHAM, H. M. Brunson

GROUP ART UNIT: 2814

9/14/02

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AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the Official Action dated January 10, 2003, please consider the remarks below and amend the above-identified patent application as follows:

IN THE SPECIFICATION

Page 42, lines 11-21, please replace the paragraph as follows:¹

In other words, the effective channel length is further increased by the shortening of the LDD length 94, compared with the first embodiment, leading to improvements in the punch-through breakdown voltage and in the short channel effect. Alternatively, since it is possible to decrease the length of the gate electrode 13, it is possible to decrease the formation area of the transistor 75, compared with the conventional high voltage PMOS

¹ A marked-up copy of the amendments is attached hereto.